# Chapter 2

# THEORY OF OPERATION

## 2.1 Introduction

This section provides a detailed theory of operation for the radio and its components.

## 2.2 Radio Power Distribution

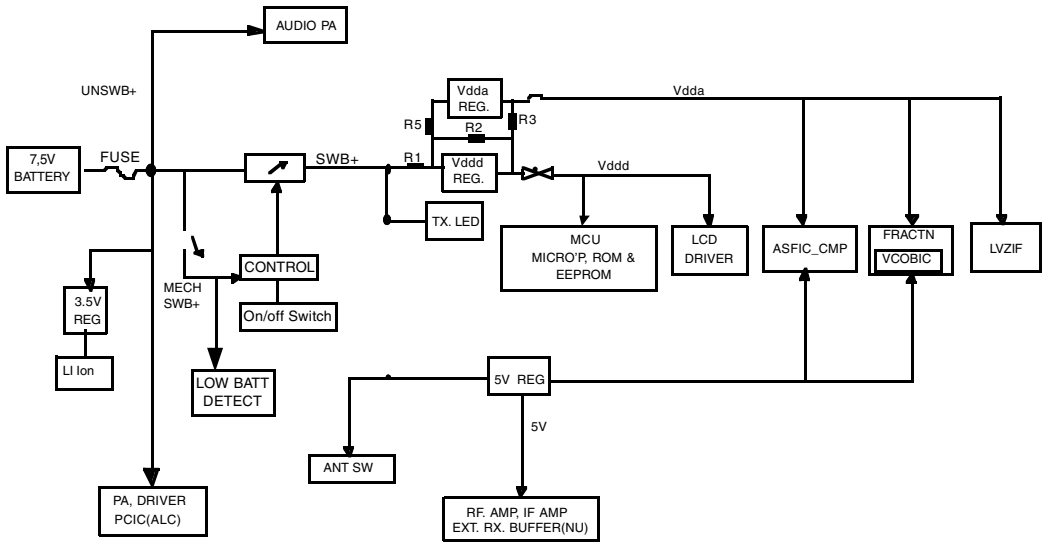



**Figure 2-1** DC Power Distribution Block Diagram

Figure 2-1 illustrates the DC power distribution throughout the radio board. A 7.5V battery (BATT 7.5V) supplies power directly to the electronic ON/OFF control as UNSWB+. When the radio is turned on, MECH_SWB+ (ON/OFF volume control) will trigger the electronic ON/OFF control (momentary-on path), then SWB+ is distributed as shown in Figure 2-1. Vdda from 3.3V Vdda regulator will then supply the microprocessor. Data is then sent to ASFIC_CMP to turn on GCB4(DAC). GCB4 will take over the momentary-on path within 12ms. SWB+ will continue to support the whole board until the radio is turned off.

Radio will be turned-off on two conditions;

1. MECH_SWB+ turned off
2. Low battery

When low battery level is detected by the microprocessor through both conditions above, it will store the radio personality data to EEPROM before turning off.

*Table 2-1. Vdd Regulator Band and Radio Jumpers*

| Jumpers | Dual Vdd Regulator Scheme | Single Vdd Regulator Scheme |
|---|---|---|
| R1 | Y | Y |
| R2 | N | N |
| R3 | N | Y |
| R4 | N | N |
| R5 | Y | N |
| Vdda | Y | N |
| SW. Reg. | N | N |

## 2.3 Keypad

The keypad block diagram is shown in Figure 2-2 Keypad Block Diagram. The LED_EN setting is set by the codeplug. When the value is set to high, the LED will not light up during power up and vice versa.

U602 is a comparator that will compare the voltage when any one of the keypad row or keypad column keys is being pressed. Therefore when a key is being pressed, it will send a message to the microprocessor through the output (KEY_INT) telling it that a key has been pressed. The microprocessor will then sample the Analog to Digital voltages at the keypad row and keypad column and map it with the table so that the key being pressed can be identified. Once the key has been identified, the message that corresponds to the key will show up at the display.

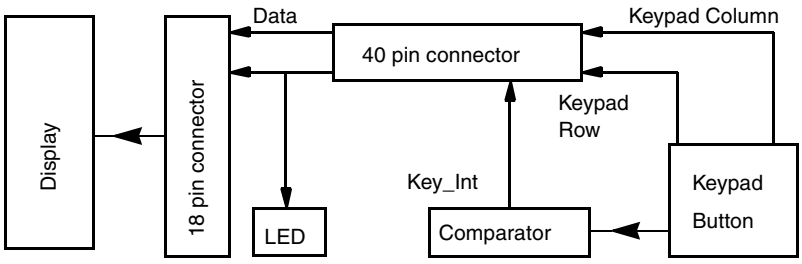



**Figure 2-2** Keypad Block Diagram

## 2.4 Controller Board

The controller board is the central interface between the various subsytems of the radio. It is separated into digital and audio architectures. The digital portion consists of a special Motorola microcontroller (HC11FL0). The audio power amplifier (Audio PA) and audio/signalling/filter/companding IC (ASFIC_CMP) form the backbone of the audio/signalling architecture.

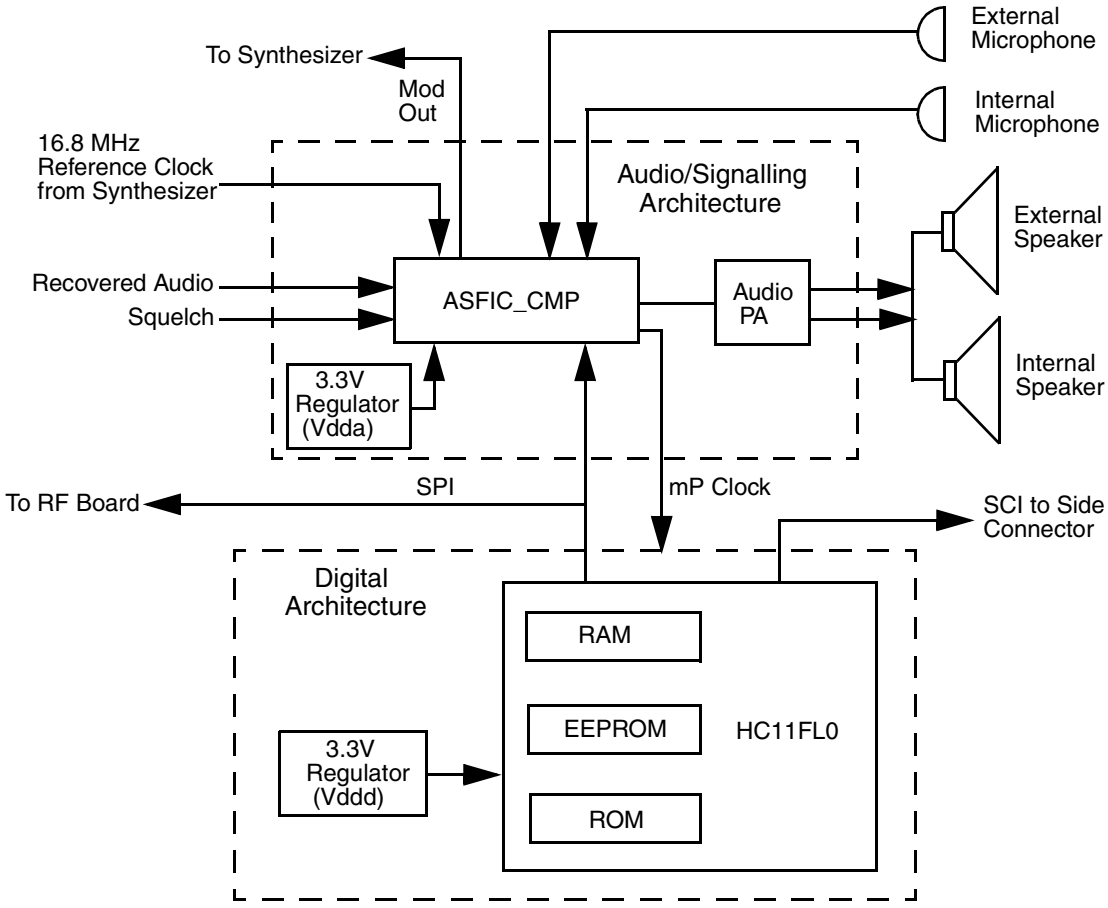



**Figure 2-3** Controller Block Diagram

### 2.4.1 MCU Configuration

There is one common MCU architecture for low-tier as well as for the high-tier products. It covers the Conventional and Trunking portables. An open architecture system with the new HC11FL0 as the processor is used. Combinations of different size RAM, ROM and EEPROM are available for various application software.

## 2.4.2 Real Time Clock (RTC)

This radio supports Real Time Clock (RTC) module for purposes of Message Time Stamping and Time Keeping. The RTC module resides in the micro-processor HC11FL0. It is kept alive by a back-up Lithium Ion battery when the primary battery is removed.

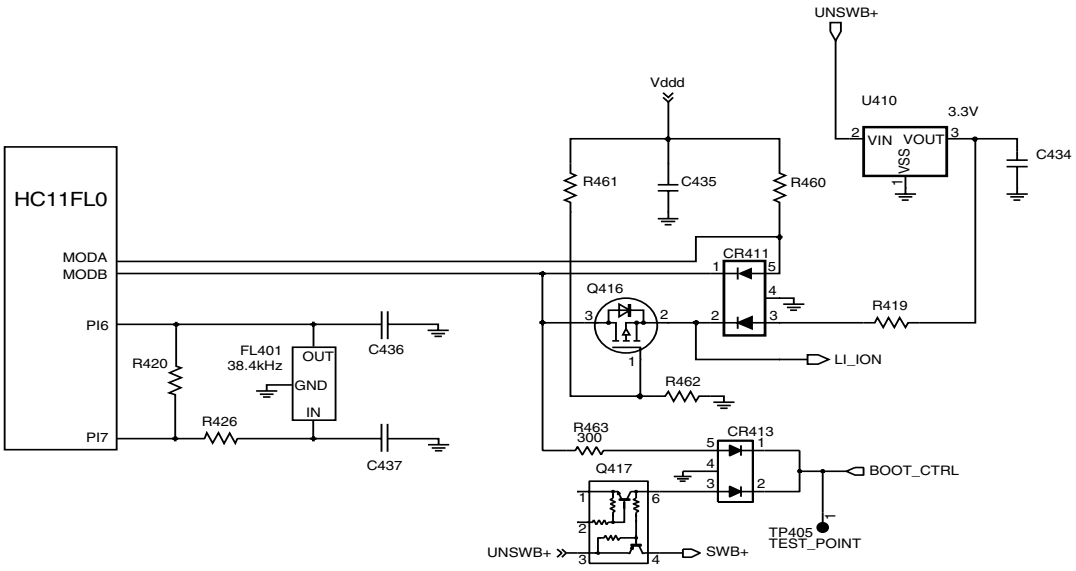



**Figure 2-4** RTC Circuit

## 2.4.3 Circuit Description

The RTC module circuit, shown if Figure 2-4, which resides in the HC11FL0 is powered by the ModB/ Vstby pin and PI6/PI7 form the crystal oscillator circuit. Clock frequency of 38.4kHz from a crystal oscillator provides the reference signal. In the processor, the frequency is divided down to 1Hz.

As the RTC module is powered separately from the processor Vdd, the RTC is kept alive through the ModB / Vstby pin when the radio is switched off. A small button Lithium Ion battery continues to feed the RTC when the primary battery is removed.

A MOSFET Q416 switches in the Li (Lithium) Ion supply when Vdd is removed. Q416 also provides isolation from BOOT_CTRL function in the event of radio program flashing. A small 3.3V regulator is used to charge the Li (Lithium) Ion battery.

### 2.4.4 ModB/Vstby Supply

The supply to the ModB/Vstby pin varies depending on the conditions listed in Table 2-2. ModB/Vstby Supply Modes

*Table 2-2. ModB/Vstby Supply Modes*

| Condition | Circuit Operation |
|---|---|
| **Radio On** | **Vdd supply voltage via CR411** |
| **Radio Off** | **• Vdd turned off**<br>**• Q416 gate is pulled low by R462**<br>**• Q416 is switched on**<br>**• U410 supplies 3.2V to ModB/Vstby** |
| **Primary battery removed** | **• Vdd turned off**<br>**• Q416 gate is pulled low by R462**<br>**• Q416 is switched on**<br>**• Li Ion battery provides 3.2V to ModB/Vstby** |
| **Flash Mode** | **• Boot_Ctrl line pull low**<br>**• ModA & ModB goes low**<br>**• Processor in boot-strap mode**<br>**• Flashing enabled** |

## 2.5 VHF Transmitter

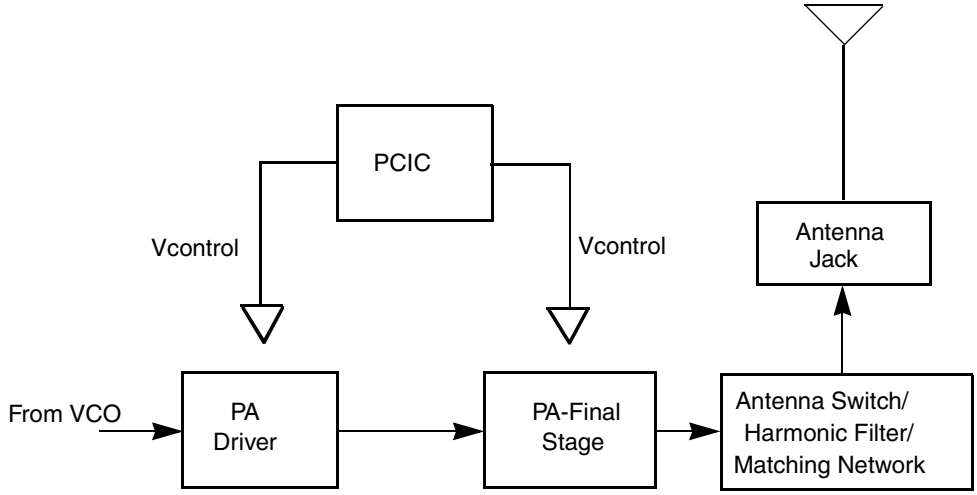



**Figure 2-5** Transmitter Block Diagram

The VHF transmitter, shown in Figure 2-5 Transmitter Block Diagram, contains five basic circuits:

- Power Amplifier
- Antenna Switch
- Harmonic Filter
- Antenna Matching Network
- Power Control Integrated Circuit (PCIC).

### 2.5.1 Power Amplifier

The power amplifier consists of two devices:

- 9Z67 LDMOS driver IC (U3501) and
- MRF1511 (P/N 4813828A08) LDMOS PA (Q3501).

The 9Z67 LDMOS driver IC contains a 2 stage amplification with a supply voltage of 7.3V.

This RF power amplifier is capable of supplying an output power of 0.3W (pin 6 and 7) with an input signal of 2mW (3dBm) (pin16). The current drain would typically be 130mA while operating in the frequency range of 136-174MHz.

The PRF1507 LDMOS PA is capable of supplying an output power of 7W with an input signal of 0.3W. The current drain would typically be 1800mA while operating in the frequency range of 136-174MHz. The power output can be varied by changing the biasing voltage.

### 2.5.2 Antenna Switch

The antenna switch circuit consists of two PIN diodes (D3521 and D3551), a pi network (C3531, L3551 and C3550), and two current limiting resistors (R3571, R3572, R3573). In the transmit mode, B+ at PCIC (U3502) pin 23 will go low and turn on Q3561 where a B+ bias is applied to the antenna switch circuit to bias the diodes “on”. The shunt diode (D3551) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

### 2.5.3 Harmonic Filter

The harmonic filter consists of C3532 to C3536, L3531 and L3532. This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. The harmonic filter insertion loss should be less than 1.2dB.

### 2.5.4 Antenna Matching Network

A matching network which is made up of L3538 and C3537 is used to match the antenna's impedance to the harmonic filter. This will optimize the performance of the transmitter and receiver into an antenna.

### 2.5.5 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U3502 to control the power output of the radio by maintaining the radio current drain. The current to the final stage of the power module is supplied through R3519 (0.1ohms), which provides a voltage proportional to the current drain. This voltage is then feedback to the Automatic Level Control (ALC) within the PCIC to keep the whole loop stable.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The voltage level is controlled by the microprocessor through the data line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C3562, C3563 and C3565) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

U3503 and its associated circuitry acts as a temperature cut back circuitry. This circuitry provides the necessary voltage to the PCIC to cut the transmitter power when the radio temperature gets too high.

## 2.6 VHF Receiver

The VHF receiver consists of a front end, back end, and automatic gain control circuits. A block diagram of the VHF receiver is shown in Figure 2-6 VHF Receiver Block Diagram. Detailed descriptions of these features are contained in the paragraphs that follow.

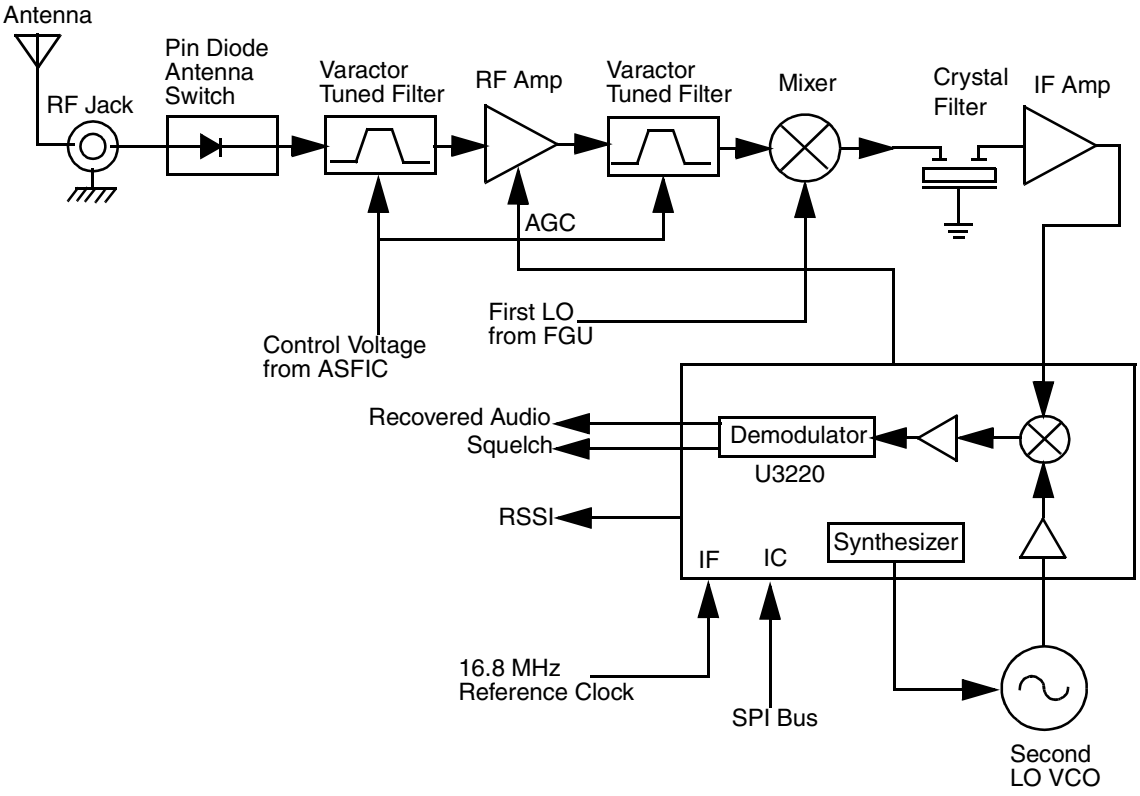



**Figure 2-6** VHF Receiver Block Diagram

### 2.6.1 Receiver Front-End

The RF signal is received by the antenna and applied to a low-pass filter. For VHF, the filter consists of L3531, L3532, C3532 to C3563. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes(D3521 and D3551) and a pi network (C3531, L3551 and C3550).The signal is then applied to a varactor tuned bandpass filter. The VHF bandpass filter comprises of L3301, L3303, C3301 to C3304 and D3301. The bandpass filter is tuned by applying a control voltage to the varactor diode (D3301) in the filter.

The bandpass filter is electronically tuned by the DACRx from IC404 which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q3302 via C3306. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L3305, L3306, C3311 to C3314 and D3302.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is about 12 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACRx.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer which consists of T3301, T3302 and CR3301. Matching of the filter to the mixer is provided by C3317,

C3318 and L3308. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using high side injection, the RF signal is down-converted to the 45.1 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (Y3200) through a resistor pad (R3321 - R3323) and a diplexer (C3320 and L3309). Matching to the input of the crystal filter is provided by C3200 and L3200. The crystal filter provides the necessary selectivity and intermediation protection.

### 2.6.2 Receiver Back-End

The output of crystal filter Y3200 is matched to the input of IF amplifier transistor Q3200 by capacitor C3203. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The gain controlled IF amplifier provides a maximum gain of about 10dB. The amplified IF signal is then coupled into U3220(pin 3) via L3202, C3207, and C3230 which provides the matching for the IF amplifier and U3220.

The IF signal applied to pin 3 of U3220 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U3220. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U3220).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U3220 so that it is very close to the first IF frequency. The IF IC (U3220) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q3270. The VCO has a varactor diode, D3270, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C3278 to C3280, R3274 and R3275.

The IF IC (U3220) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the front-end.

The demodulated signal on pin 27 of U3220 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

### 2.6.3 Automatic Gain Control Circuit

The front end automatic gain control circuit provides automatic reduction of gain, of the front end RF amplifier via feedback. This action is necessary to prevent overloading of back end circuits. This is achieved by drawing some of the output power from the RF amplifier output. At high radio frequencies, capacitor C3327 provides the low impedance path to ground for this purpose. CR3302 is a PIN diode used for switching the path on or off. A certain amount of forward biasing current is needed to turn the PIN diode on. Transistor Q3301 provides this current.

Radio signal strength indicator, RSSI, a voltage signal, is used to drive Q3301 to saturation i.e. turned on. RSSI is produced by U3220 and is proportional to the gain of the RF amplifier and the input power to the radio.

Resistors R3304 and R3305 are voltage dividers designed to turn on Q3301 at certain RSSI levels. In order to turn on Q3301 the voltage across R3305 must be greater or equal to the voltage across R3324, plus the base-emitter voltage (Vbe) present at Q3301. Capacitor C3209 is used to dampen any instability while the AGC is turning on. The current flowing into the collector of Q3301, a high current gain NPN transistor, will be drawn through the PIN diode to turn it on. Maximum current

flowing through the PIN is limited by the resistors R3316, R3313, R3306 and R3324. C3326 is a feedback capacitor used to provide some stability to this high gain stage.

An additional gain control circuit is formed by Q3201 and its associated circuitry. Resistors R3206 and R3207 are voltage dividers designed to turn on Q3201 at a significantly higher RSSI level than the level required to turn on PIN diode control transistor Q3301. In order to turn on Q3201 the voltage across R3207 must be greater or equal to the voltage across R3208, plus the base-emitter voltage (Vbe) present at Q3201. As current starts flowing into the collector of Q3201, it reduces the bias voltage at the base of IF amplifier transistor Q3200 and in turn, the gain of the IF amplifier. The gain can be controlled in a range of -30dB up to +10dB.

### 2.6.4 Frequency Generation Circuitry

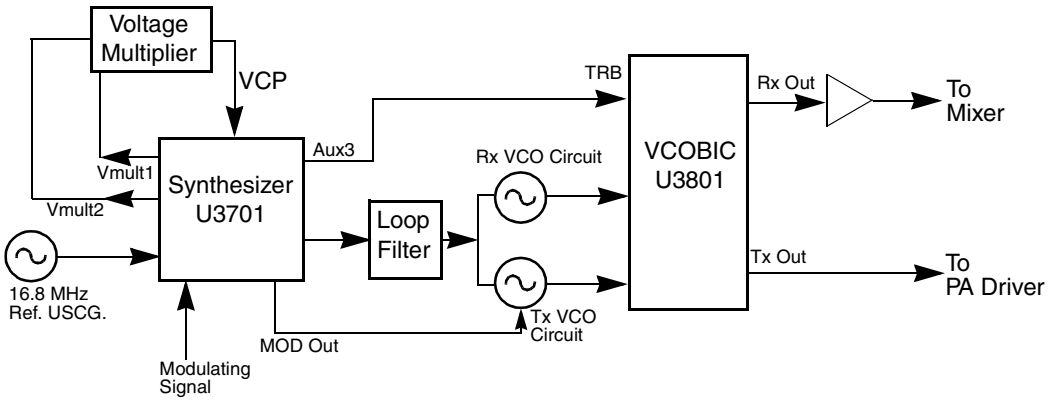



**Figure 2-7** Frequency Generation Unit Block Diagram

The Frequency Generation Circuitry, shown in Figure 2-7 Frequency Generation Unit Block Diagram, is composed of two main ICs, the Fractional-N synthesizer (U3701), and the VCO/Buffer IC (U3801). Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5V and 3.3V which come from U3711 and U3201 respectively. The synthesizer in turn generates a superfiltered 4.5V which powers U3801.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U3701. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

## 2.7 Synthesizer

The Fractional-N Synthesizer, shown in Figure 2-8 Synthesizer Block Diagram, uses a 16.8MHz crystal (Y3761) to provide a reference for the system. The LVFractN IC (U3701) further divides this to 2.1MHz, 2.225MHz, and 2.4MHz as reference frequencies. Together with C3761, C3762, C3763, R3761 and D3761, they build up the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8MHz at pin 19 of U3701 to be used by ASFIC and LVZIF.

The loop filter which consist of C3721, C3722, R3721, R3722 and R3723 provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U3701 to put synthesizer within the lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier which is made up of C3701 to C3704 and triple diodes D3701, D3702. Two 3.3V square waves (180 deg out of phase) are first multiplied by four and then shifted, along with regulated 5V, to build up 13.5V at pin 47 of U3701.

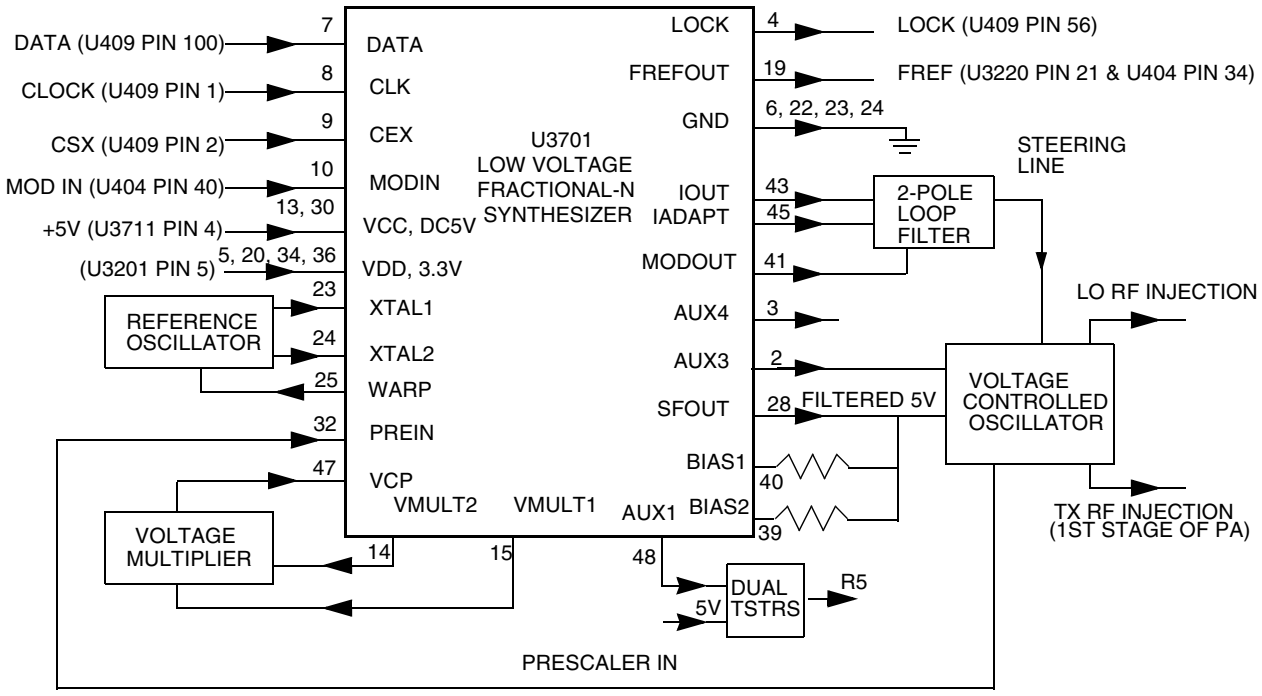



**Figure 2-8** Synthesizer Block Diagram

## 2.8 Voltage Controlled Oscillator (VCO)

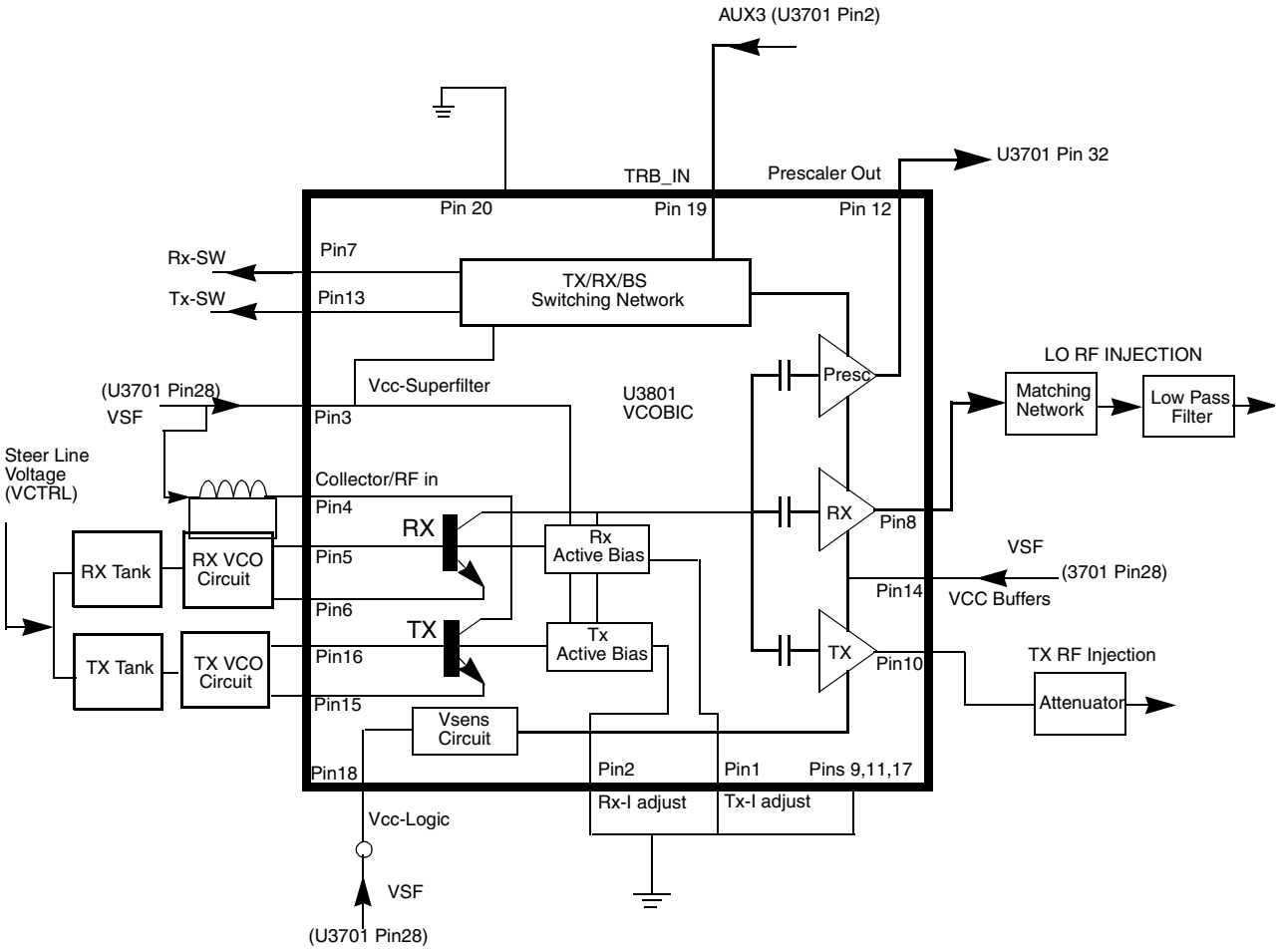



**Figure 2-9** VCO Block Diagram

The VCOBIC (U3801), shown in Figure 2-9 VCO Block Diagram, in conjunction with the Fractional-N synthesizer (U3701) generates RF in both the receive and the transmit modes of operation. The TRB line (U3801 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U3801 pin 12, through a low pass filter, to the prescaler input (U3701 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage typically between 3.5V and 9.5V when the PLL is locked on frequency.

The RF section of the VCOBIC(U3801) is operated at 4.54 V (VSF), while the control section of the VCOBIC and Fractional-N synthesizer (U3701) is operated at 3.3V. The operation logic is shown in Table 2-3..

*Table 2-3. VCO Control Logic*

| Desired Mode | AUX 4 | AUX 3 | TRB |
|---|---|---|---|
| **Tx** | **n.u.** | **High (@3.2V)** | **High (@3.2V)** |
| **Rx** | **n.u.** | **Low** | **Low** |
| **Battery Saver** | **n.u.** | **Hi-Z/Float (@1.6V)** | **Hi-Z/Float (@1.6V)** |

In the receive mode, U3801 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U3801. The RF signal at U3801 pin 8 is run through a matching network. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at T3302.

During the transmit condition, when PTT is depressed, 3.2 volts is applied to U3801 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U3801. The RF signal at U3801 pin 10 is injected into the input of the PA module (U3501 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through U3701 pin 41.

When a high impedance is applied to U3801 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

## 2.9 UHF Transmitter (Band 1 and Band 2)

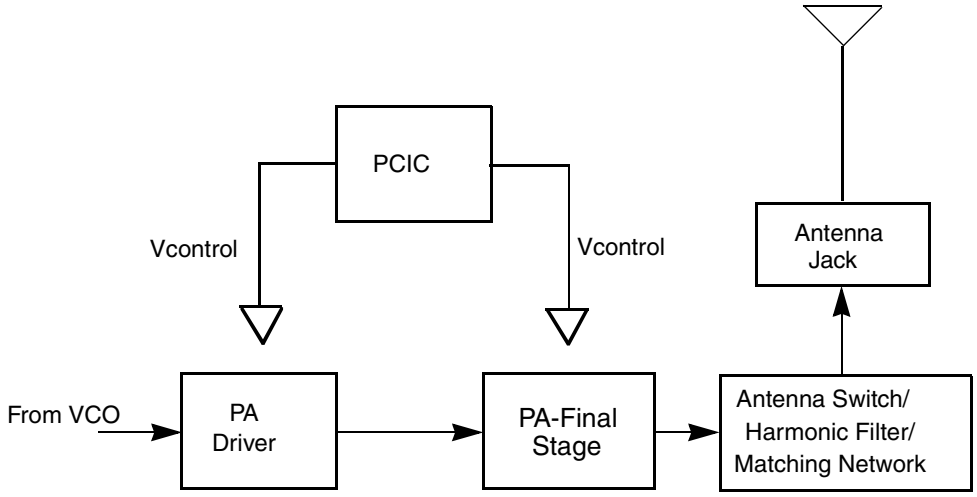



**Figure 2-10** Transmitter Block Diagram

The UHF transmitter consists of the following basic circuits as shown in Figure 2-10

- Power Amplifier
- Antenna Switch
- Harmonic Filter
- Antenna Matching Network
- Power Control Integrated Circuit (PCIC).

### 2.9.1 Power Amplifier

The power amplifier consists of two devices:

- 9Z67 LDMOS driver IC (U101) and
- MRF1517 (P/N 4813828A09) LDMOS PA (Q110).

The 9Z67 LDMOS driver IC contains a 2 stage amplification with a supply voltage of 7.3V.

This RF power amplifier is capable of supplying an output power of 0.3W (pin 6 and 7) with an input signal of 2mW (3dBm) (pin16). The current drain would typically be 160mA while operating in the frequency range of 403-470MHz for Band 1 or 450-527MHz for Band 2.

The PRF1507 LDMOS PA is capable of supplying an output power of 7W with an input signal of 0.3W. The current drain would typically be 1300mA while operating in the frequency range of 403-470MHz for Band 1 or 450-527MHz for Band 2. The power output can be varied by changing the biasing voltage.

### 2.9.2 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C107, L104 and C106), and two current limiting resistors (R101, R170). In the transmit mode, B+ at PCIC (U102) pin 23 will go low and turn on Q111 where a B+ bias is applied to the antenna switch circuit to bias the diodes “on”. The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

### 2.9.3 Harmonic Filter

The harmonic filter consists of C104, L102, C103, L101 and C102. The design of the harmonic filter for UHF is that of a modified Zolotarev design. It has been optimized for efficiency of the power module. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2dB.

### 2.9.4 Antenna Matching Network

A matching network which is made up of L116 is used to match the antenna's impedance to the harmonic filter. This will optimize the performance of the transmitter and receiver into an antenna.

### 2.9.5 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R101, which provides a voltage proportional to the current drain. This voltage is then fedback to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C133, C134 and C135) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

CR105 and its associated components are part of the temperature cut back circuitry. It senses the printed circuit board temperature around the transmitter circuits and output a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

## 2.10 UHF Receiver (Band 1 and Band 2)

The UHF receiver consists of a front end, back end, and automatic gain control circuits. a block diagram of the receiver is shown in Figure 2-11 UHF Receiver Block Diagram. Detailed description of

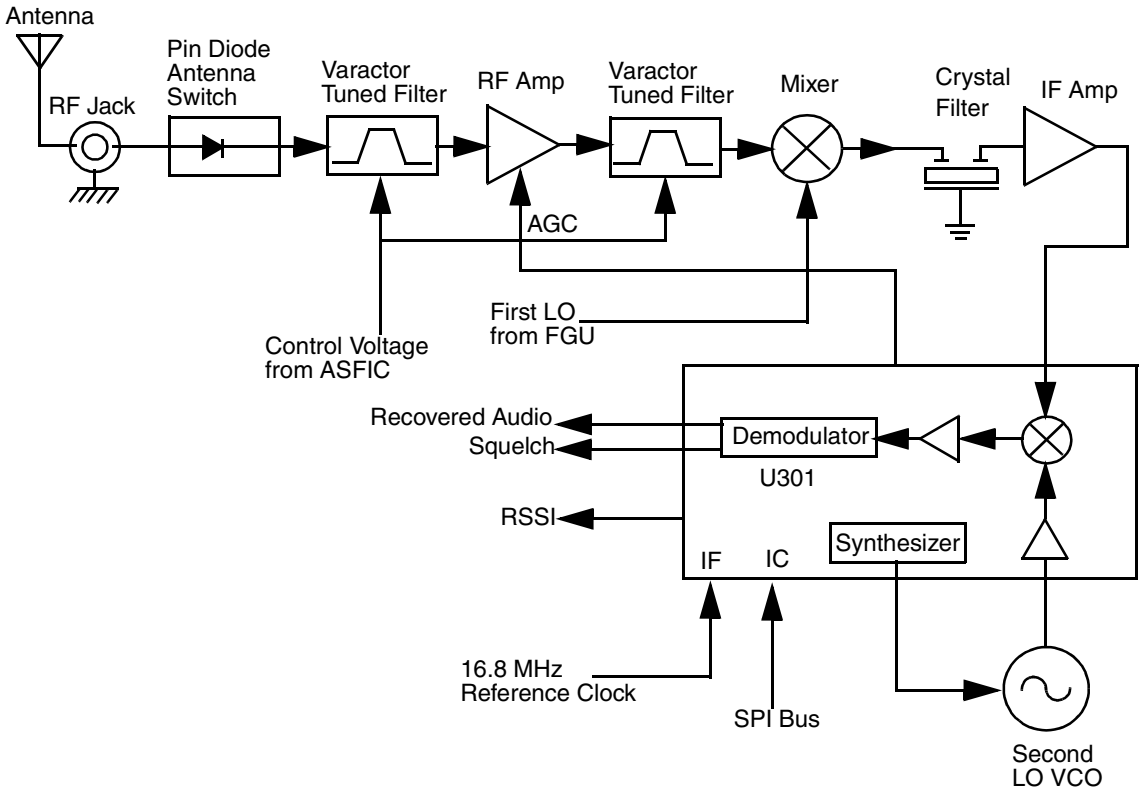



**Figure 2-11** UHF Receiver Block Diagram

these stages are contained in the paragraphs that follow.

### 2.10.1 Receiver Front-End

The RF signal is received by the antenna and applied to a low-pass filter. For UHF, the filter consists of L101, L102, C102, C103, C104. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes(CR101 and CR102) and a pi network (C106, L104 and C107).The signal is then applied to a varactor tuned bandpass filter. The UHF bandpass filter comprises of L301, L302, C302, C303, C304, CR301 and CR302. The bandpass filter is tuned by applying a control voltage to the varactor diodes(CR301 and CR302) in the filter.

The bandpass filter is electronically tuned by the DACRx from IC404 which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q301 via C307. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L306, L307, C313, C317, CR304 and CR305.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is about 50 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACRx.

The output of the post-RF amplifier filter which is connected to the passive double balanced mixer consists of T301, T302 and CR306. Matching of the filter to the mixer is provided by C381. After

mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 45.1 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL301) through a resistor pad and a diplexer (C322 and L310). Matching to the input of the crystal filter is provided by C324 and L311. The crystal filter provides the necessary selectivity and intermodulation protection.

## 2.10.2 Receiver Back-End

The output of crystal filter FL301 is matched to the input of IF amplifier transistor Q302 by components R352 and C325. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The IF amplifier provides a gain of about 7dB. The amplified IF signal is then coupled into U301(pin 3) via C330, C338 and L330 which provides the matching for the IF amplifier and U301.

The IF signal applied to pin 3 of U301 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U301. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U301).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U301 so that it is very close to the first IF frequency. The IF IC (U301) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q320. The VCO has a varactor diode, CR310, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C362, C363, C364, R320 and R321.

The IF IC (U301) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the front-end.

The demodulated signal on pin 27 of U301 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

## 2.10.3 Automatic Gain Control Circuit

The front end automatic gain control circuit is to provide automatic gain reduction of the front end RF amplifier via feedback. This action is necessary to prevent overloading of back end circuits. This is achieved by drawing some of the output power from the RF amplifier’s output. At high radio frequencies, capacitor C331 provides the low impedance path to ground for this purpose. CR308 is a PIN diode used for switching the path on or off. A certain amount of forward biasing current is needed to turn the PIN diode on. Transistors Q315 provides this current where upon saturation, current will flow via R347, PIN diode, collector and emitter of Q315 and R319 before going to ground. Q315 is an NPN transistor used for switching here. Maximum current flowing through the PIN is mainly limited by the resistor R319.

Radio signal strength indicator, RSSI, a voltage signal, is used to drive Q315 to saturation hence turning it on. RSSI is produced by U301 and is proportional to the gain of the RF amplifier and the input RF signal power to the radio.

Resistor network at the input to the base of Q315 is scaled to turn on Q315, hence activating the AGC, at certain RSSI levels. In order to turn on Q315, the voltage across the transistor’s base to ground must be greater or equal to the voltage across R319, plus the base-emitter voltage (Vbe) present at Q315. The resistor network with thermistor RT300 is capable of providing temperature compensation to the AGC circuit, as RSSI generated by U301 is lower at cold temperatures

compared to normal operation at room temperature. Resistor R300 and capacitor C397 form an R-C network used to dampen any transient instability while the AGC is turning on.

### 2.10.4 Frequency Generation Circuitry

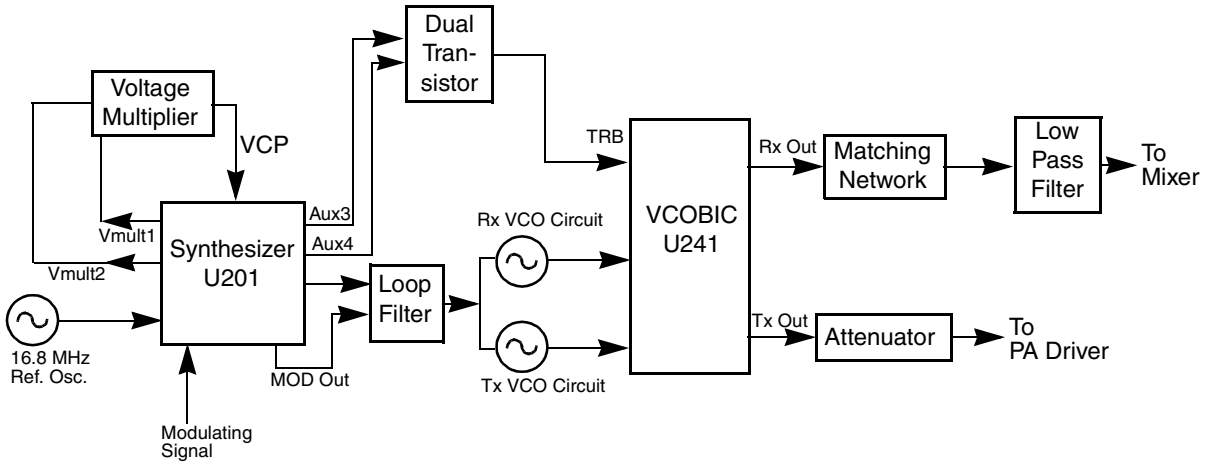



**Figure 2-12** Frequency Generation Unit Block Diagram

The Frequency Generation Circuitry is composed of two main ICs, the Fractional-N synthesizer (U201), and the VCO/Buffer IC (U241). Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5V and 3.3V which come from U247 and U248 respectively. The synthesizer in turn generates a superfiltered 4.5V which powers U241.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U201. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

## 2.11 Synthesizer

The Fractional-N Synthesizer uses a 16.8MHz crystal (FL201) to provide a reference for the system. The LVFractN IC (U201) further divides this to 2.1MHz, 2.225MHz, and 2.4MHz as reference frequencies. Together with C206, C207, C208, R204 and CR203, they build up the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8MHz at pin 19 of U201 to be used by ASFIC and LVZIF.

The loop filter which consist of C231, C232, C233, R231, R232 and R233 provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put synthesizer within the lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier which is made up of C258, C259, C228, triple diode CR201 and level shifters U210 and U211. Two 3.3V

square waves (180 deg out of phase) are first shifted to 5V, then along with regulated 5V, put through arrays of diodes and capacitors to build up 13.3V at pin 47 of U201.

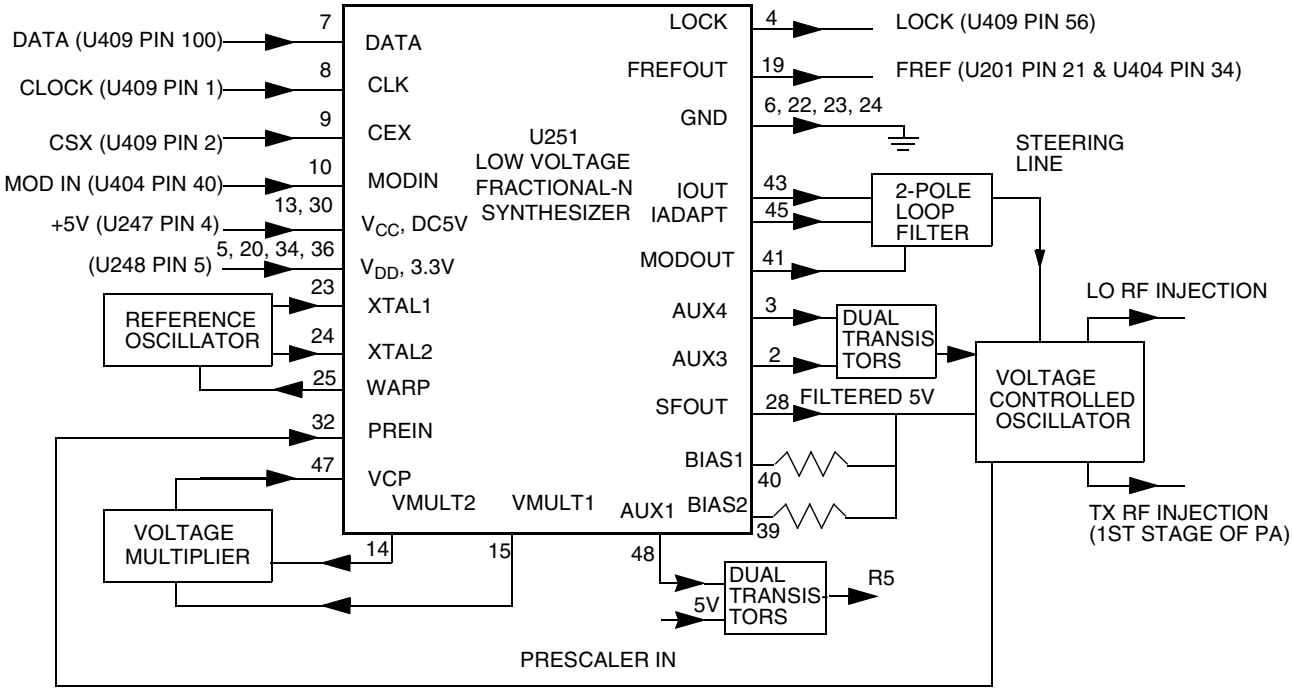



**Figure 2-13** Synthesizer Block Diagram

## 2.12 Voltage Controlled Oscillator - (VCO)

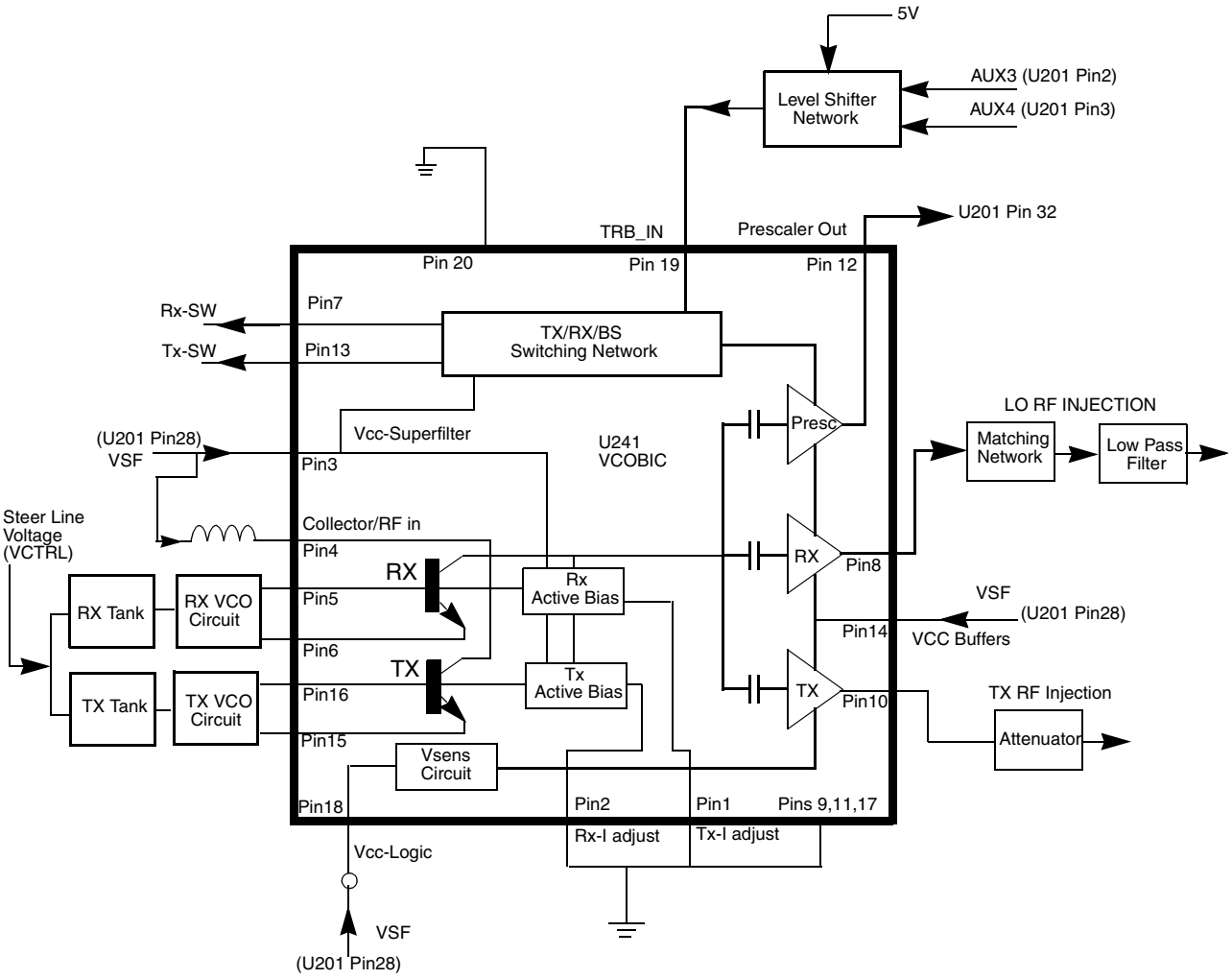



**Figure 2-14** VCO Block Diagram

The VCOBIC (U241) in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U241 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U241 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 3.5V and 9.5V when the PLL is locked on frequency.

The VCOBIC(U241) is operated at 4.54 V (VSF) and Fractional-N synthesizer (U201) at 3.3V. This difference in operating voltage requires a level shiftier consisting of Q260 and Q261 on the TRB line.

The operation logic is shown notable Table 2-4. Level Shifter Logic.

*Table 2-4. Level Shifter Logic*

| Desired Mode | AUX 4 | AUX 3 | TRB |
|---|---|---|---|
| **Tx** | **Low** | **High (@3.2V)** | **High (@4.8V)** |
| **Rx** | **High** | **Low** | **Low** |
| **Battery Saver** | **Low** | **Low** | **Hi-Z/Float (@2.5V)** |

In the receive mode, U241 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U241. The RF signal at U241 pin 8 is run through a matching network. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at T302.

During the transmit condition, when PTT is depressed, five volts is applied to U241 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U241. The RF signal at U241 pin 10 is injected into the input of the PA module (U101 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U241 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.